

SPECIFICATIONS FOR OLED MODULE

MODEL NO.
BL2004AM-ERNJU20I\$
VER.01



FOR MESSRS:

ON DATE OF:

APPROVED BY:

BOLYMIN, INC.

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BOLYMIN

1. Numbering System

B	L	2004	AM	-	E	R	N	J	U	20I	\$	
0	1	2	3		4	5	6	7	8	9	10	11

0	Bolymin	B											
1	Module Type	L	OLED										
2	Format	2004	20 character type,4lines										
3	Version No.	AM											
		-											
4	LCD Color	L	OLED/Green					E	OLED/Yellow				
		W	OLED/White					R	OLED/RED				
		K	OLED/BLUE										
5	LCD Type	R	Positive/reflective										
6	Backlight type/color	N	No backlight										
7	CGRAM Font	J	English/Japanese Font					E	English/European Font				
		B	English/Japanese/European					C	English/Cyrillic Font				
8	View Angle /Operation Temperature	U	6:00/Ultra wide Temperature					H	6:00 /Wide Temperature				
9	Special Code	3	3 voltage logic power supply					N	Positive voltage for LCD				
		20K	RS 232 I/F					20C	I2C I/F				
		20I	SPI I/F										
		68K	6800 mode,4-bits					80J	8080 mode,8-bits				
		80K	8080 mode,4-bits										
10	RoHS	\$											
11	Customer Code	<u>00</u> 0 ~ <u>99</u> 0 、 <u>AA</u> 0 ~ <u>ZZ</u> 0											

2.General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of Characters	20 characters× 4 Lines	dots
Module dimension (L*W*H)	98.0 x 60.0 x 13.1	mm
View area	76.0 x 24.2	mm
Active area	70.42 x 20.82	mm
Dot size	0.57 x 0.57	mm
Dot pitch	0.60 x 0.60	mm
Character size (L x W)	2.97 x 4.77	mm
Character pitch (L x W)	3.55 x 5.35	mm

(2) Controller IC: Compatible with PT0066

IC Equivalent (compatible) HD44780, KS0066 , SPLC780 , ST7066 , AIP31066

3.Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operating Temperature	TOP		-40	---	+80	°C
Storage Temperature	TST		-40	---	+90	°C
Supply Voltage(Logic)	VDD		-0.3	---	5.5	V
Input Voltage	VI		-0.3	---	5.5	V
Operating life time		80cd/m ²	---	100000	---	Hrs

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.

Note 3: Ta = 25°C, 25% Checkerboard.

Software configuration follows section actual application example Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions..

4. Electrical Characteristics

(Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)	VDD	—	2.8	5.0	5.3	V
Input High Vol	V _{IH}	—	0.7V _{DD}	—	V _{DD}	V
Input Low Vol	V _{IL}	—	0	—	0.3V _{DD}	V
Output High Vol	V _{OH}	—	0.7V _{DD}	—	V _{DD}	V
Output Low Vol.	V _{OL}	—	—	—	0.3V _{DD}	V
Supply Current (*)	IDD	—	—	40	—	mA

Note : VDD=5.0V, 25% Display Area Turn on 100 cd/m².

When random texts pattern is running, averagely, about 1/4 of pixels will be on.

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	—	Free	—	deg
Dark Room contrast	>10000:1			—
CIE x,y (Color: Yellow)	(0.46,0.45)	(0.50,0.49)	(0.54,0.53)	
Brightness	—	100	—	cd/m ²

6.Interface Pin Function

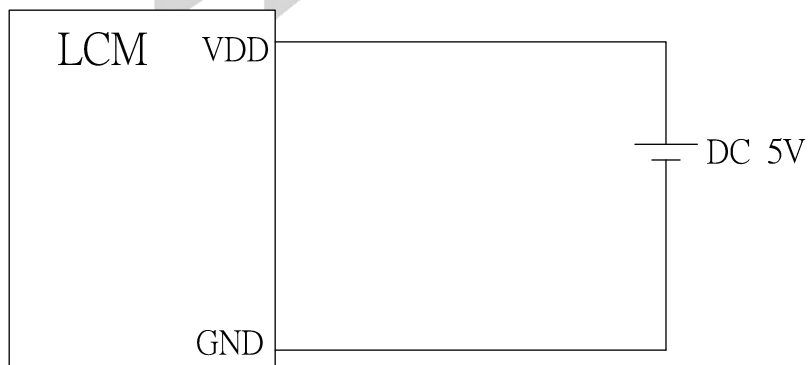
IF1:

1	GND	0V	Ground
2	VDD	5.0V	Supply Voltage for logic.
3	NC	-	No connection
4	RS	H/L	This is the Data/Command control pad that determines whether the data bits are data or a command. RS = "H":treated as display data. RS = "L":transferred to the command registers.
5	NC	-	No connection.
6	NC	-	No connection.
7	SCL	H/L	Serial clock input
8	SI	H/L	Serial data input
9	NC	-	No connection.
10	NC	-	No connection.
11	NC	-	No connection.
12	NC	-	No connection.
13	NC	-	No connection.
14	NC	-	No connection.
15	NC	-	No connection
16	NC	-	No connection

※SPI Series Interface is Default

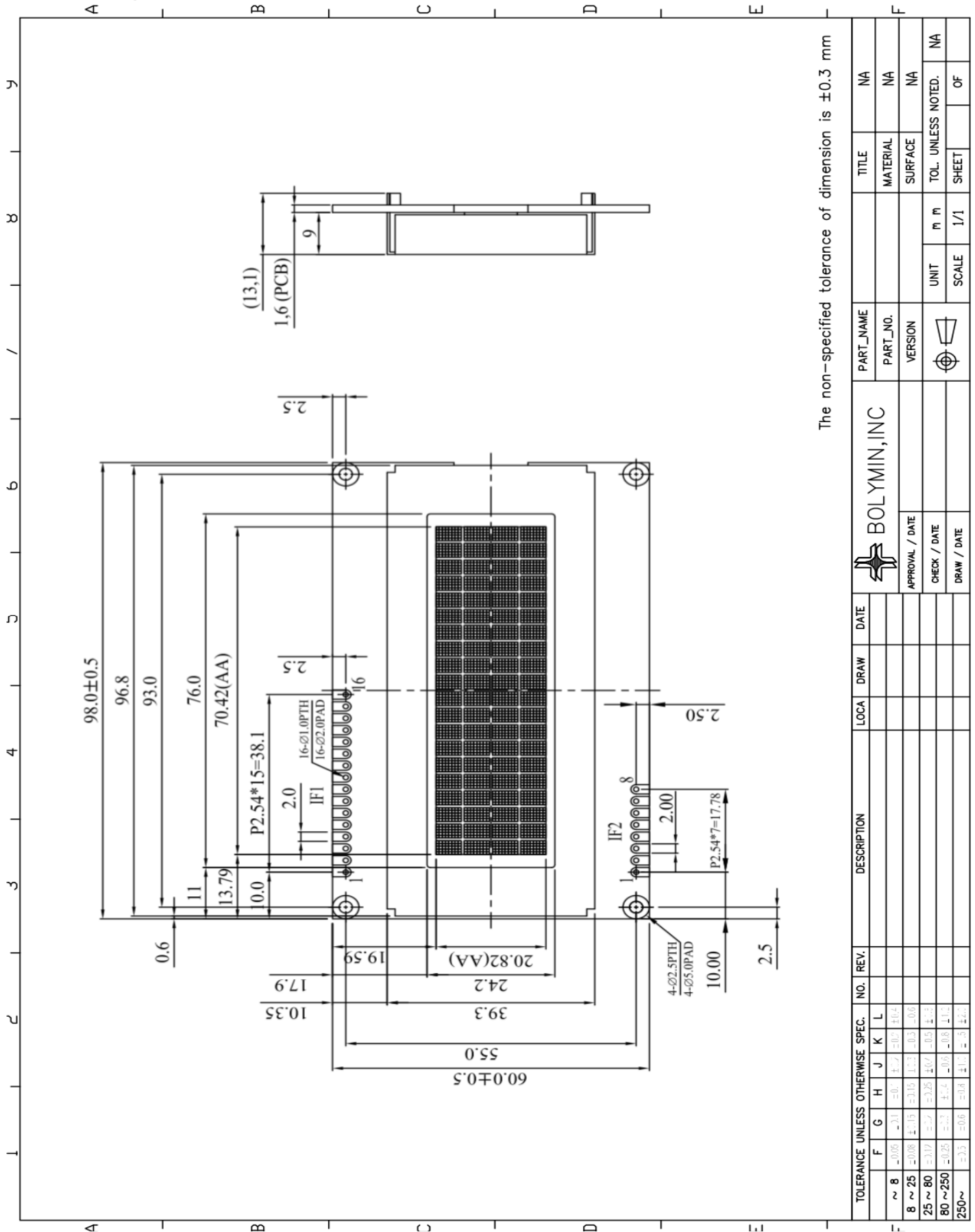
7.Power supply for LCD Module

* LCM operating on "DC 5.0V " input with built-in positive voltage



8.Drawing& Block Diagram

8.1 Drawing



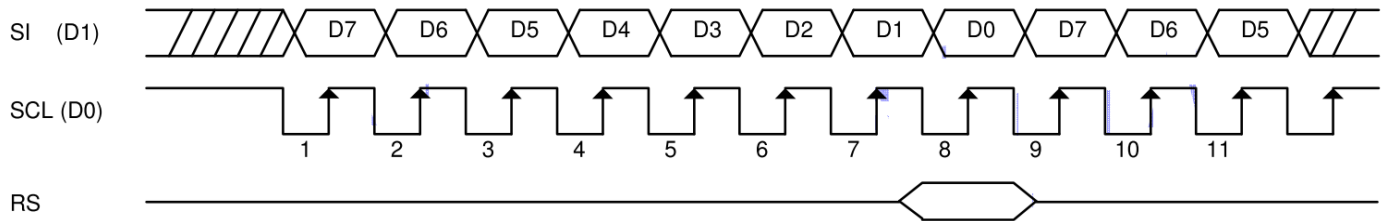
The non-specified tolerance of dimension is ± 0.3 mm

TOLERANCE UNLESS OTHERWISE SPEC.		NO.		REV.		DESCRIPTION		LOCA	DRAW	DATE	BOLYMIN, INC		PART_NAME		TITLE	
F	G	H	J	K	L						APPROVAL / DATE		PART_NO.	MATERIAL	NA	
$\sim B$	± 0.05	± 0.1	± 0.15	± 0.2	± 0.3						CHECK / DATE		VERSION	SURFACE	NA	
$8 \sim 25$	± 0.08	± 0.15	± 0.2	± 0.3	± 0.5						DRAW / DATE				NA	
$25 \sim 80$	± 0.12	± 0.2	± 0.25	± 0.3	± 0.5										TOL. UNLESS NOTED.	
$80 \sim 250$	± 0.25	± 0.3	± 0.4	± 0.5	± 0.8										NA	
$250 \sim$	± 0.3	± 0.6	± 0.8	± 1.0	± 1.5										NA	
												UNIT	m	m		
												SCALE	1/1			
												SHEET	1/1	OF		

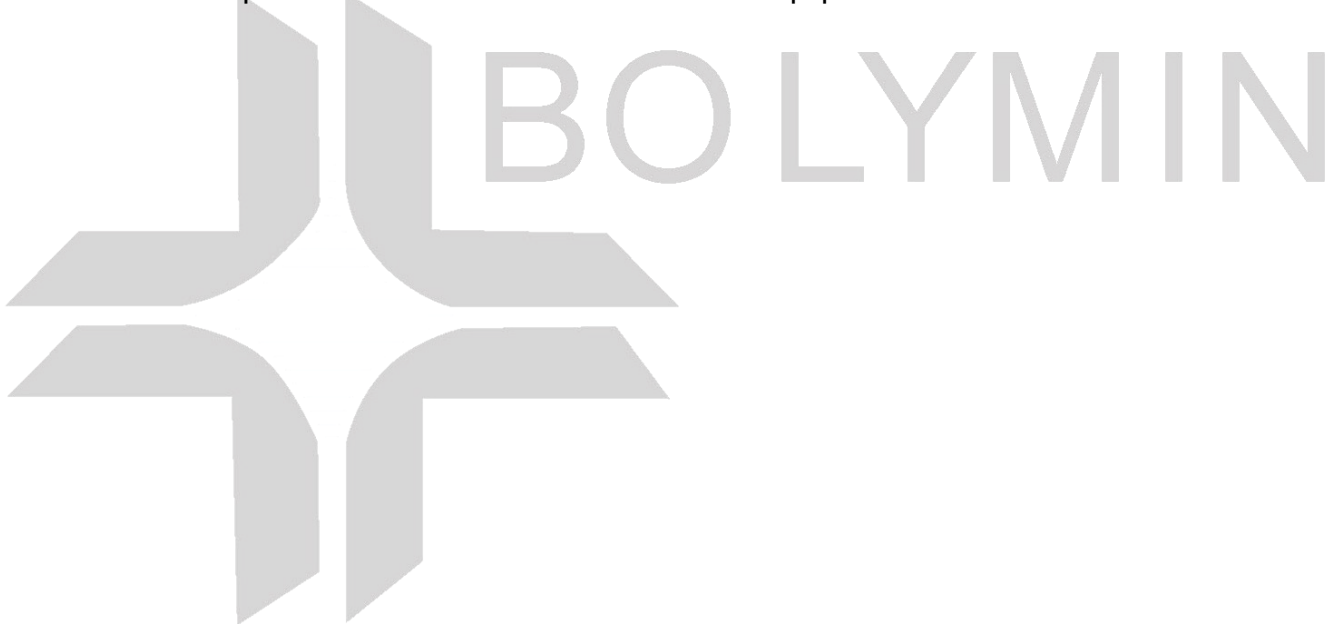
9. Controller Data

9.1 4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, RS. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock.

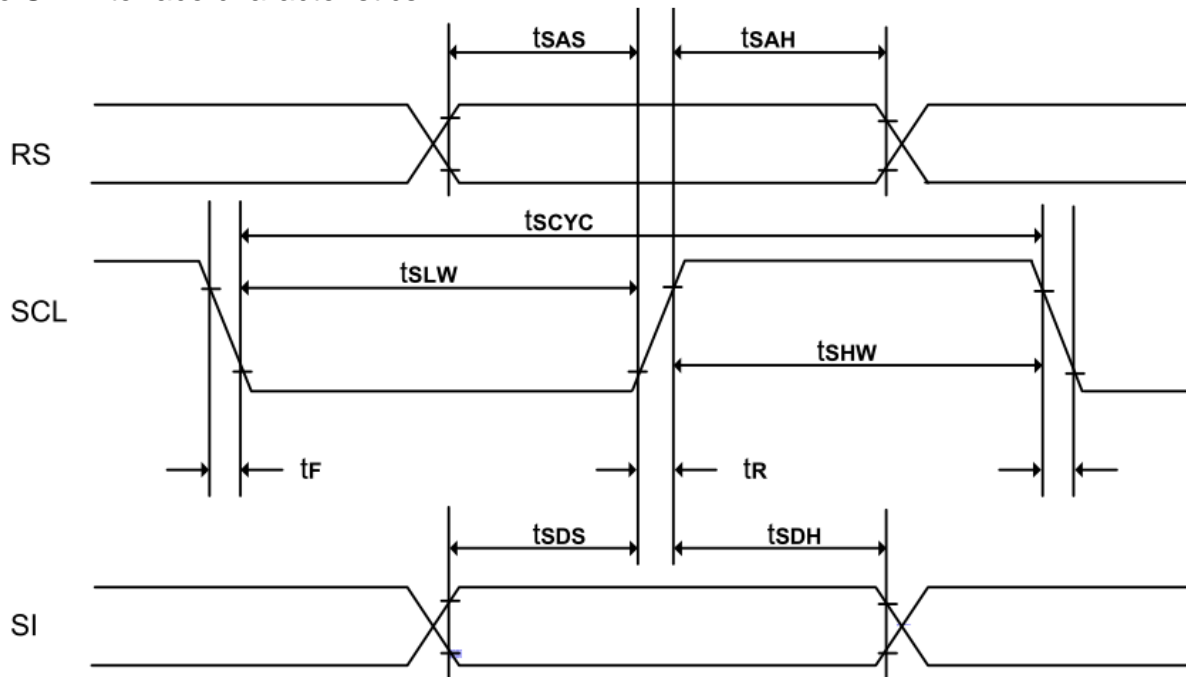


- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.



9.2 System buses Read/Write Characteristics

4-wire SPI interface characteristics



	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

9.3 Display Control Instruction

Instruction	Instruction Code										Description	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display area.(POR = 01H)	
Return Home	0	0	0	0	0	0	0	0	0	1	Counter with DDRAM address 00H. (POR = 10H)	
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.(POR = 08H)
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Shift display or move cursor..
Function Set	0	0	0	0	1	DL	N	F	—	—	—	Set number of display line (N), and character font (F). (POR = 30H)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	—	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	—	Set DDRAM address in address counter.
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	—	Read Busy Flag (BF) and Address Counter (POR = 00H)
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	—	Write data to CG RAM or DD RAM. (POR= 00H)
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	—	Read data from CG RAM or DD RAM. (POR = 00H)

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

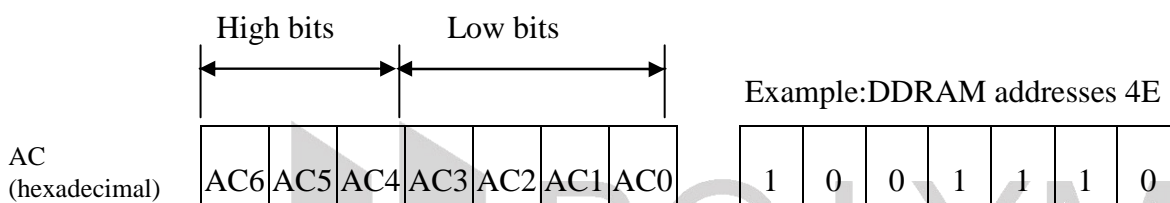
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80x8 bits or 80 characters. Below figure is the relationship between DDRAM addresses and positions on the liquid crystal display.



DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	14	16
00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

Example: 1-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5x8 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5x8 dots, eight character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

10. Built-in CGROM (Character Generator ROM)

ENGLISH_JAPANESE

Upper 4bit Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
0001	CG RAM (2)	タ	チ	ツ	テ	ト	ナ	ニ	ノ	ネ	ヌ	ナ	ニ	ノ	ネ	ヌ
0010	CG RAM (3)	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ
0011	CG RAM (4)	ハ	ヒ	フ	ヘ	ホ	マ	ミ	ム	メ	モ	ヤ	ユ	ユ	ヨ	ヨ
0100	CG RAM (5)	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ	タ	チ	ツ	テ	ト
0101	CG RAM (6)	ナ	ニ	ノ	ネ	ヌ	フ	フ	フ	フ	フ	ハ	ヒ	フ	ヘ	ホ
0110	CG RAM (7)	マ	ミ	ム	メ	モ	ヤ	ユ	ユ	ヨ	ヨ	カ	キ	ク	ケ	コ
0111	CG RAM (8)	サ	シ	ス	セ	ソ	タ	チ	ツ	テ	ト	ナ	ニ	ノ	ネ	ヌ
1000	CG RAM (1)	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ
1001	CG RAM (2)	ハ	ヒ	フ	ヘ	ホ	マ	ミ	ム	メ	モ	ヤ	ユ	ユ	ヨ	ヨ
1010	CG RAM (3)	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ	タ	チ	ツ	テ	ト
1011	CG RAM (4)	ナ	ニ	ノ	ネ	ヌ	フ	フ	フ	フ	フ	ハ	ヒ	フ	ヘ	ホ
1100	CG RAM (5)	マ	ミ	ム	メ	モ	ヤ	ユ	ユ	ヨ	ヨ	カ	キ	ク	ケ	コ
1101	CG RAM (6)	サ	シ	ス	セ	ソ	タ	チ	ツ	テ	ト	ナ	ニ	ノ	ネ	ヌ
1110	CG RAM (7)	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ	フ
1111	CG RAM (8)	ハ	ヒ	フ	ヘ	ホ	マ	ミ	ム	メ	モ	ヤ	ユ	ユ	ヨ	ヨ